VIDEO CONFERENCING INTERFACE

This application claims the benefit of U.S. Provisional Application
No. 60/094,646, filed 30 July 1998.

TECHNICAL FIELD

This invention relates to video conferencing systems and, more specifically, to a
system which interfaces with one or more of a plurality of video input and one or more
of a plurality of output devices.

BACKGROUND

Video conferencing systems are typically designed for use with one particular
type of video input device, such as an NTSC camera ("NTSC" means the North
American and Japanese analog video standard), a PAL camera ("PAL" means the
European analog video standard), a digital camera, or a high speed serial interface
camera (*e.g.*, a FireWire or Universal Serial Bus (USB) camera). Such systems are also
typically designed for use with one particular output device, such as an NTSC or PAL
video monitor, a television set, a Liquid Crystal Display (LCD) screen, or a computer
monitor.

Systems having an interface for video conferencing systems that allow the users
or manufacturers of such systems to intermingle video input and output devices as they
choose, or as a particular video conferencing application dictates, rather than being
required are not known. That is, existing systems are believed to require a particular
video input device and a particular output device dictated by the video signal formal for
the selected video conferencing system.

DISCLOSURE OF INVENTION

A video conferencing interface is part of a standards-based video conferencing
system with excellent video and audio quality, high compression, and great flexibility,
all at a low cost. The interface includes an Application Specific Integrated Circuit
(ASIC) that incorporates a unique blend of computation and data path designs
implemented in hardware, as well as processing and control developed for flexibility
using a standard processor.

The "hybrid" method of computation and control available in the disclosed
system provides an advantage over "single solution" counterparts in which computation
and control is implemented in dedicated hardware only. The use of dedicated hardware

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only leads to relative inflexibility in bit rate control. The "hybrid" method of computation and control in the disclosed system provides and an advantage over counterparts that use a software-programmed processor only, thereby abandoning the speed advantages of a hardware implementation.

5   The disclosed system employs hardware to implement or provide for computation and for a data path to provide for high speed data processing at a much faster rate than could be done in a processor-only environment (*i.e.*, software). A standard software based processor allows for flexibility of control so the system can be made adaptable for several different configurations. However, the result is a slower

10   speed because of the software configuration. To attain higher speeds using hardware, a separate hardware configuration would be needed for each variation needed leading to considerable cost and complexities for implementation.

For example, it is often desirable to control the bit rate at which the system interface processes images so an appropriate balance can be struck between the quality of the images processed, on the one hand, and the speed with which images are

15   processed, on the other hand. When rapid motion occurs in the processed images, for example, it is typically desirable to operate at an increased bit rate so that the rapid motion is quickly processed and communicated. However, the high speed processing negatively impacts image quality. When the images to be processed are relatively

20   static from image to image (*e.g.*, frame to frame), it typically is desirable to operate at a reduced bit rate, but with increased image quality. In a hardware-only implementation, such flexibility would have to be hardwired at greater expense, or would simply be unavailable. In a software-only implementation, flexibility is maintained, but at the expense of reduced processing speed. The present invention employs a "hybrid"

25   approach, heretofore unknown, to secure the benefits of a fixed hardware and a fixed software solution.

In the described embodiment of the present invention, the ASIC is the key to implementing this hybrid approach. The ASIC provides a hardwired implementation for computation and data movement while also providing the flexibility inherent in

30   processor-based processing and control.

In addition to the ASIC, the system incorporates a memory to store the video information as it is being compressed and/or displayed. The system also includes

memory and Electrically Erasable Programmable Read Only Memory (EEPROM) for instructions and data storage for the processor, audio input and output, and a MOdulator/DEModulator (MODEM) for telephone/network interface. (The EEPROM and MODEM are actually optional depending on the configuration requirements.)

5   The ASIC also includes several interfaces that are flexible in their function that allow for several different system configurations with minimal modification or cost impact. These interfaces include the video input, the video output, and the high speed serial interface.

10   BRIEF DESCRIPTION OF DRAWINGS

In the drawings:

FIG. 1 is a block diagram depiction of a basic ASIC of the prior art suitable for use in processing video signals;

FIG. 2 is a block diagram of the ASIC suitable for use in one form of a video

15   system of the present invention;

FIG. 3 is is a block diagram of the ASIC suitable for use in another form of a video system of the present invention;

FIG. 4 is a block diagram of a high speed serial interface circuit for use with a video system of the present invention;

20   FIG. 5. is a block diagram of a video input block of an ASIC used with a video system of the present invention;

FIG. 6 is a block diagram of a bus control block of an ASIC used with a video system of the present invention; and

FIG. 7. is a block diagram of a video output block of an ASIC used with a video

25   system of the present invention.

BEST MODES FOR CARRYING OUT THE INVENTION

As shown in Figure 1, a conventional ASIC 10 may be included on a circuit board 12 . The circuit board 12 includes a memory 14 connected to a Memory Control

30   30 forming a memory module 15 that functions to retain video signals. Memory 14 may be implemented as a dynamic random access memory (DRAM), a static random

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access memory (SCRAM), or other suitable memory device architecture known by persons skilled in the art.

The circuit board 12 may also have an optional EEPROM module 16. A separate processor memory module 18 (*e.g.*, SCRAM DRAM, etc.) along with an audio

5   input/output (I/O) module 20 (connected, for example, to a microphone or speaker), and a MODEM and/or Network interface (*e.g.*, LAN or local area network interface) module 22 which together function as a remote video interface circuit 19 may also be included on the circuit board 12.

In one operational configuration, Video-In circuitry 24 receives digital video

10   signals 26 from a single or selected video signal source. "H.263" is a video compression/decompression standard established by the International Telecommunications Union (ITU). H.263 Encode circuitry 34 directs the Memory Control circuitry 30 to forward stored digital video data sent to it from the video memory module 15. The Memory Control circuitry 30 sends the stored video data that

15   it receives out onto and along the memory bus 32. As the H.263 Encode circuitry 34 encodes (*i.e.*, compresses) the stored digital video data, it passes the now encoded digital video data to a MODEM or a Network module 22 for transmission to a remote station (not shown) at which location the digital video data may be decoded and subsequently displayed for viewing by a user. The remote station may include the

20   inventive video conferencing interface described herein, or it may be a conventional video conferencing system interface.

Encoded digital video data is transmitted by and also received from the remote station or another station through the MODEM or the Network 22. The MODEM or the Network 22 transmit and receive data. If a MODEM is used, the signal is

25   modulated and or demodulated and transmitted over an appropriate line such a telephone line or any equivalent thereof. Alternately, it may be transmitted through a network wiring arrangement which is configured to provide video signal transmission.

The data received from the remote location through a MODEM, a network or what ever else may be extant, is transferred through the Processor circuitry 40 to the

30   Bus Control circuitry 36. The Bus Control Circuitry 36 passes the data over the data bus 38 to H.263 Decode circuitry 42 for decoding. After decoding the digital video data, the H.263 Decode circuitry 42 forwards the decoded digital video data to the

Memory Control circuitry 30 over the memory bus 32 for storage in the DRAM 14.
Video Out circuitry 44 then directs the Memory Control circuitry 30 to retrieve the
stored digital video data from the DRAM 14 for output by the Video Out circuitry 44 in
digital form for display by a selected video display device (not shown) connected to

5   receive the video signal from the Video Out Circuitry 44.

Alternatively, serial digital video data, or serial control signals from an attached
computer system, can be input or output through high speed serial interface circuitry 46,
as will be described in more detail below.

Support circuitry 48 and performs certain "housekeeping" and control

10   functions. The Support circuitry 48 interacts with the EEPROM module 16 via a well-
known I²C bus 50, handling interrupt signals, INT, and reset signals, RST, and
programming an array of programmable I/O pins, PIO (not shown).

The EEPROM module 16 may be used to store machine code for the operation
of the Processor circuitry 40. At start-up, the machine code can be transferred from the

15   relatively slow EEPROM module 16 to the relatively fast processor memory device 18
for use by the Processor circuitry 40 during normal operations.

The system of the present invention shown in FIG. 2 incorporates a plurality of
video input options supplied by video input means 11 the output of which is supplied as
the input video signal 26. The input means 11 is here shown to include two or more

20   sources of video signals. The sources illustrated include an Internal Digital Camera 52,
an Internal NTSC or PAL video camera 56, an External NTSC or PAL video Camera
58. Input may also be had from an External High Speed Serial Camera 60. Although
shown separated from the input means 11, the High Speed Serial Camera 60 can be
incorporated into the input means 11 or positioned separately to supply an input signal

25   to the data bus 38.

An "internal" camera 52 is a camera in which the lens and interface control are
mounted inside the system enclosure, while an "external" camera interfaces through a
connector which may be the video decoder 54.

More specifically, as shown in Figure 2, the digital video signals 26 can be

30   generated by the internal digital camera 52, or by the Video Decoder module 54
converting analog NTSC or PAL signals from the internal NTSC or PAL camera 56 or
the external NTSC or PAL camera 58 to the digital video signals 26. Alternatively, or

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in addition, a digital camera 60 having a high speed serial output, such as a FireWire or

USB port, can output serial digital video signals to the high speed serial interface 46 for

further processing and transmission to the data bus 38.

The ASIC 10 of FIG. 2 is configured to have a memory means 15 that includes

5   the DRAM 14 and the memory control 30. Memory control circuitry 30 transfers the

digital video signals 26 from a memory bus 32 to the DRAM 14 for storage and also to

the H.263 encode module 34 for compression prior to processing by the video

processing means 35. The video processing means 35 includes the Processor 40 as

well as the support circuit 48 and the bus control 36. It also includes the processor

10   Memory 18 and the EEPROM 16 if provided.

The video processing means 35 and more specifically the Processor circuitry 40

directs the encoded digital video data to the remote interface circuit 19. The remote

interface circuit 19 is any suitable circuit to transmit and receive video conferencing

signals to and from a remote source. That is, the remote interface circuit 19 is

15   configured to receive video signals and preferably voice signals from a remote source to

effect what may be referred to as video conferencing. The outgoing video signals as

well as audio signals are sent to a remote location which ideally is returning similar

video signals and audio signals for processing by the ASIC and for presentation as a

video signal on a selected video display or output device. The remote interface means

20   19 is here illustrated to include the MODEM 22 and Audio circuit 20.

The ASIC 10 of FIG. 2 has all the other processing circuitry of FIG. 1 as shown

in FIG. 2 while at the same time differing significantly in that a plurality of video input

arrangements can be accepted from the video input means 11 using a combination of

software and hardware to facilitate speed in processing and flexibility.

25   The system of the present invention in another embodiment depicted in FIG. 3

may also integrate one of several video output options, including NTSC/PAL 68, a

Video Modulator 62, LCD 72, RGB 71, and a remote device connected by conductors

73 through the High Speed Serial Interface 46.

More specifically, as shown in Figure 3, the digital video output of the Video

30   Out circuitry 44 can be provided to video output means 43 which is here shown to

include a Video Modulator module 62 to convert the digital video output from the

video out circuitry 44 to a modulated analog signal 64. The analog signal is then

multiplexed by a Cable Multiplexer module 66 for output as a TV channel (e.g., channel "3") to a monitor 68. Alternatively, the digital video output of the Video Out circuitry 44 can be converted by a Video Encoder module 70 to an NTSC or PAL analog format suitable for input to a dedicated port on the monitor 68, or can be

5   converted into an LCD format signal for an LCD screen 72. In still another alternative, the Video Encoder module 70 can convert the digital video output from the Video Out circuitry 44 to an RGB signal 71 suitable for direct application to a computer monitor (not shown).

The system of the present invention can be configured or modified through the

10   specific use of the High Speed Serial Interface 46 connected to separate video 47 not illustrated in FIG. 3. The video means 47 (FIG. 4), can be used for video input, and/or video output. Additionally, it can be used to connect the system as a peripheral or remote device to another controller. This controller could be, for example, a cable box, a set top box, a personal computer, or any number of general purpose or task specific

15   controller devices. Likewise, this also allows the system to easily be integrated directly into a stand-alone teleconferencing device or video phone.

More specifically, as shown in Figure 4, the depicted ASIC 10 has a High Speed Serial Interface circuit 46 (e.g., a FireWire or USB port) which outputs serial digital video data 71 to video means 47. The video means 47 may include a controller with

20   modem 74, which then interfaces with the telephone system 76 or a separate monitor such as monitor 68.

As shown in Figure 5, the Video-In circuitry 24 includes Input Configuration circuitry 78 that receives digital video signals 26, as well as serial digital video data from the data bus 38. Control register circuitry 80 set by the Bus Control circuitry 36

25   (see Figure 2) causes the Input Configuration circuitry 78 to select and output either the signals 26 or the data from the data bus 38 in a 4:2:2 YUV format. Pixel Decimation circuitry 82 then reduces the "color" component of the output signal, thereby reducing the data density of the signal, by outputting the signal in a 4:1:1 YUV format. Then, a First-In-First-Out (FIFO) buffer 84 holds the output signal before transferring it to the

30   memory means 15 via memory bus 32.

As shown in Figure 6, the Bus Control circuitry 36 includes Bone Interface circuitry 86 for receiving data from the data bus 38 (otherwise known as the

"backbone") and Processor Interface circuitry 88 which communicates with the

Processor circuitry 40 (*see* Figure 4). Arbitration and Control circuitry 90 selects which

Interface circuitry 86 and 88 will be active at any one time, and Host Interface circuitry

92 communicates data internally to and from the selected Interface circuitry 86 or 88.

5   Data from the Host Interface circuitry 92 proceeds to Data Interface Control circuitry

94, while register information proceeds to Register Interface Control circuitry 96. Both

of the circuitry 94 and 96 communicate with Third Party Module circuitry 98, such as

FireWire or USB serial-to-parallel circuitry.

As shown in Figure 7, the Video Out circuitry 44 includes Memory

10   Control/Sequencer circuitry 100 that directs the Memory Control circuitry 30 (*see*

Figure 1) to provide it with digital video data from the Video Memory module 14 (*see*

Figure 1) in the proper sequence. Line Store circuitry 102 then acts as a buffer for

storing the video data until two video lines of data are stored. Interpolator circuitry 104

then reverses the actions of the Pixel Decimation circuitry 82 (*see* Figure 5) by

15   interpolating between each two lines of video data it receives to generate a 4:2:2 YUV

signal. A storage FIFO buffer 106 then stores the interpolated video data, and Control

Registers circuitry 108 controlled by the Bus Control circuitry 36 (*see* Figure 1) then

causes Encoder Control circuitry 110 to output the stored video data, or not, as the

situation may dictate. At the same time, the stored video data is provided on the data

20   bus 38 to the Bus Control circuitry 36 (Figure 1) for use by the High Speed Serial

Interface circuitry 46 (*see* Figure 1).

The systems of FIGS. 2 or 3 can be easily and inexpensively configured as

several different devices including, but not limited to: a PC peripheral for camera or

video conferencing; a cable box peripheral for camera or video conferencing; and a

25   remote camera for surveillance systems. In addition, the system that includes the circuit

of FIGS. 2 or 3 can be integrated into or tightly coupled with other hardware to create

other devices including, but not limited to, a set top box video conferencing system; a

cable box video conferencing system; and a video phone.

It should be understood, of course, that the systems depicted in Figures 2-7 may

30   be a transmitting or receiving station, or, more likely in most video conferencing

systems, both.

The embodiments herein illustrated and described are not intended to limit the scope of the invention as defined in the following claims.